What is Claimed is:

[c1] A method for forming a transistor, the method comprising the steps of:
a) providing a semiconductor substrate;
b) providing an epitaxial layer on a substrate;
b) providing a dopant source layer on the epitaxial layer;
c) diffusing dopant from the dopant source layer into the epitaxial layer, said dopant diffusion forming at least a portion of an extrinsic base for the transistor.

[c2] The method of claim 1 wherein the dopant source layer comprises a doped single crystal layer formed on the epitaxial layer.

[c3] The method of claim 2 wherein the dopant source layer is doped between $5x10^{19}$ and $1x10^{21}$ atoms/cm^3.

[c4] The method of claim 1 further comprising the step of implanting into epitaxial layer, the implanting forming a second portion of the extrinsic base for the transistor.

[c5] The method of claim 1 further comprising the step of forming a pedestal on the epitaxial layer, and wherein the dopant source layer is formed around the such that the pedestal defines a portion of the epitaxial layer in which the dopant source layer is not formed on the epitaxial layer.

[c6] The method of claim 5 wherein the pedestal further defines an emitter opening.

[c7] The method of claim 5 wherein the step of forming a pedestal comprises forming a high pressure oxide layer, a nitride layer, and an oxide layer, and patterning the high pressure oxide layer, nitride layer and oxide layer.

[c8] The method of claim 5 wherein the step of forming a pedestal comprises depositing and patterning an oxide layer.

[c9] The method of claim 1 wherein the dopant source layer comprises a raised portion of the extrinsic base.

[c10] A method for forming bipolar transistor on a semiconductor substrate, the

method comprising the steps of:

a) providing a semiconductor substrate;

b) forming an epitaxial layer on the semiconductor substrate;

c) forming a pedestal on epitaxial layer, the pedestal defining an emitter region of the epitaxial layer;

d) forming a dopant source layer on the epitaxial layer, the dopant source layer not formed on the epitaxial layer where the pedestal is on the epitaxial layer;

e) diffusing dopant from the dopant source layer and into the epitaxial layer to form at least a portion of an extrinsic base.

[c11] The method of claim 10 wherein the epitaxial layer comprises silicon germanium.

[c12] The method of claim 10 wherein the step of forming a pedestal comprises forming a high pressure oxide layer, a nitride layer, and an oxide layer, and patterning the high pressure oxide layer, nitride layer and oxide layer.

[c13] The method of claim 10 wherein the step of forming a pedestal comprises depositing and patterning an oxide layer.

[c14] The method of claim 10 wherein the dopant source layer comprises a raised portion of the extrinsic base.

[c15] The method of claim 10 further comprising the step of implanting into epitaxial layer, the implanting forming a second portion of the extrinsic base for the transistor.

[c16] The method of claim 10 wherein the dopant source layer is self-aligned to the pedestal.

[c17] A transistor formed on a semiconductor substrate, the bipolar transistor comprising;

b) an epitaxial layer on the semiconductor substrate;

b) a dopant source dopant source layer on the epitaxial layer;

c) dopants from the dopant source layer diffused into the epitaxial layer to form at least a portion of the extrinsic base for the bipolar transistor.

[c18] The transistor of claim 17 wherein the dopant source layer comprises a doped single crystal layer formed on the epitaxial layer.

[c19] The transistor of claim 17 wherein the epitaxial layer comprises a silicon germanium layer.

[c20] The transistor of claim 17 the dopant source layer is doped between $5x10^{19}$ and $1x10^{21}$ atoms/cm^3.

[c21] The transistor of claim 17 wherein the dopant source layer comprises a raised portion of the extrinsic base that is coupled to the dopants diffused from the dopant source layer.